Physique d'acquisition d'images

Capteurs d'images - Jérôme Vaillant
Imagerie non-conventionnelle et co-conception – Corinne Fournier

Agenda

- (Brief) Introduction to image sensors
  - The ubiquitous CMOS image sensor
  - Smartphone camera: a co-design system
- What is a pixel?
  - How does it work
  - Design and fabrication
  - Optical elements
  - Implementation in a matrix
  - Noises
- Un-conventional / non-visible pixels
  - Depth sensing with pixels
  - Infrared pixels

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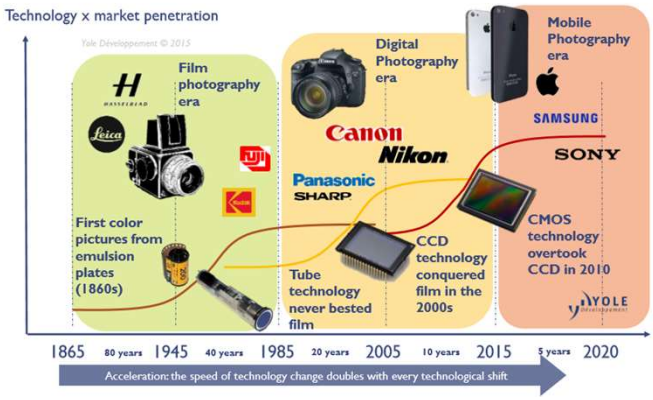
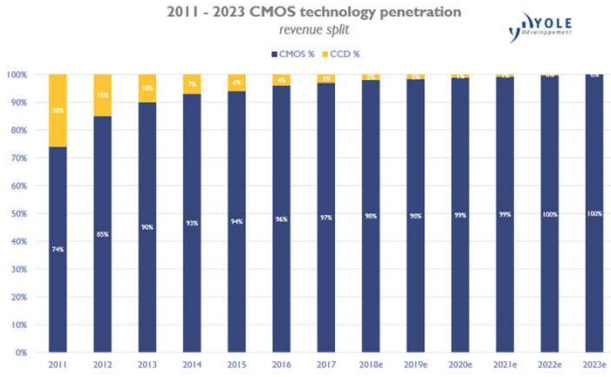
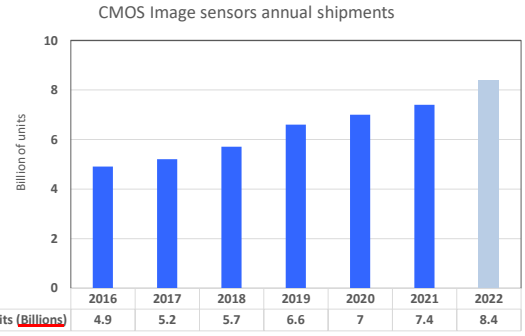
What's (CMOS) image sensor?

- Array of transductors (pixels) converting photons to electrons
  - CCD: merely a matrix of pixels only => electronics is outside the chip
  - CMOS: integrated circuit
- Brief history:



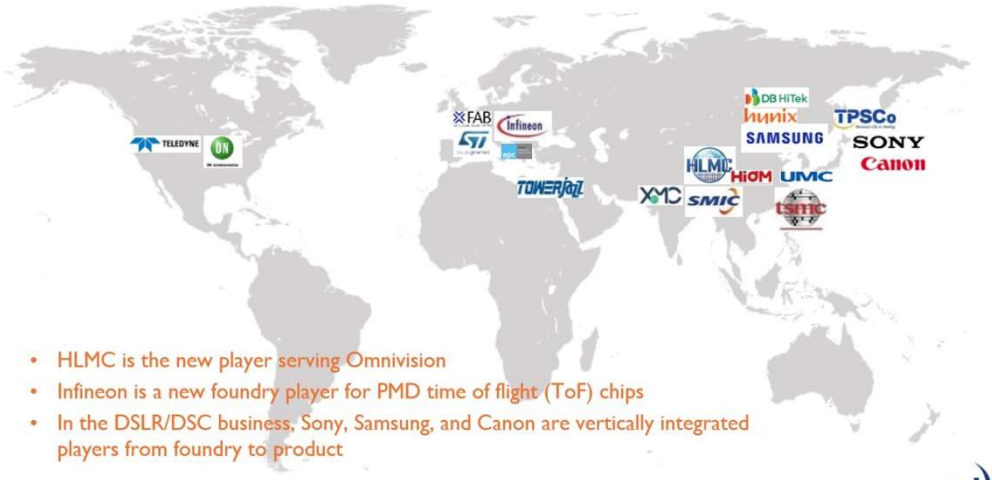


CMOS image sensors today



Units (Billions)	2016	2017	2018	2019	2020	2021	2022
	4.9	5.2	5.7	6.6	7	7.4	8.4

IMAGE SENSOR FOUNDRIES - GEOGRAPHIC MAPPING



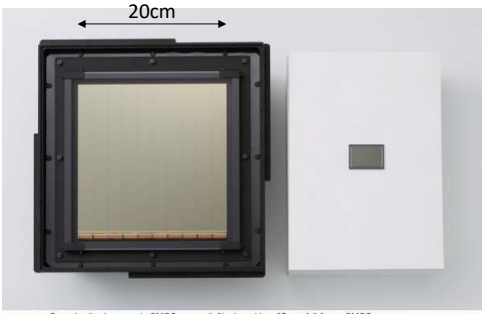
- HLMC is the new player serving Omnivision
- Infineon is a new foundry player for PMD time of flight (ToF) chips
- In the DSLR/DSC business, Sony, Samsung, and Canon are vertically integrated players from foundry to product

YOLE Développement

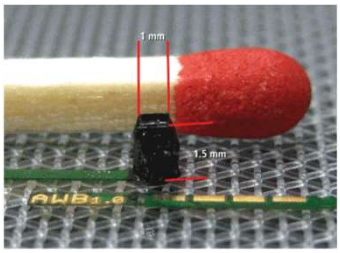
| Status of the CIS industry| www.yole.fr | ©2018

Overview of pixels zoology

- Pixel size from 200µm down to 0.61µm !
- Image definition from 0.3Mpix to 120Mpix
- Image sensor surface from <2x1.5mm² up to 200x200mm²



Canon's ultra-large-scale CMOS sensor (left) alongside a 35 mm full-frame CMOS sensor



AWAIBA 250x250-pixel NanEye for medical applications

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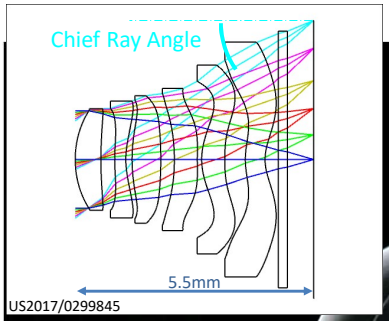
A camera in less than 1 cm^3

Optimized objective



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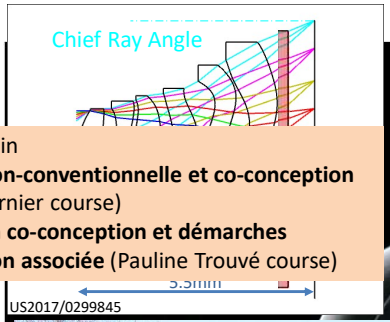
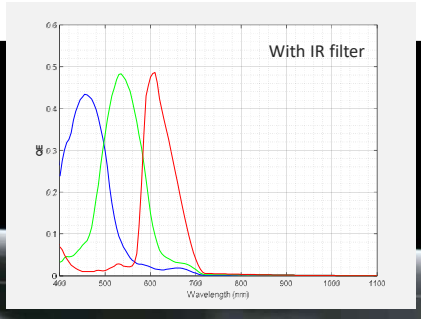
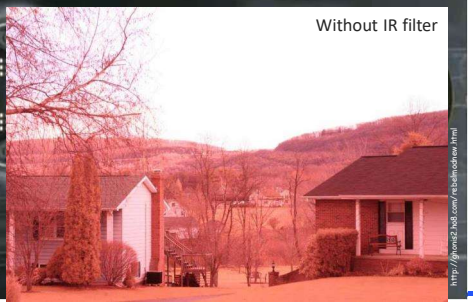
Optimized objective with IR cut filter



More details in
- **Imagerie non-conventionnelle et co-conception** (Corinne Fournier course)
- **Modèles en co-conception et démarches d'optimisation associée** (Pauline Trouvé course)

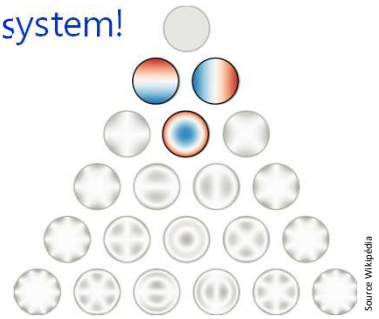
US2017/0299845





Smartphone camera: a basic adaptive optics system!

- Modern cameras are 3-modes AO systems
  - Optical Image Stabilization (OIS) is a tip-tilt corrector
  - Autofocus is a defocus corrector



- Extended Depth of Focus (eDoF) uses wavefront coding and image deconvolution
  - Introduction of phase plate in objective
  - PSF with low dependence in z, but enlarged in x,y (image plane)
  - *New paradigm for imaging systems*, Cathey et al., https://doi.org/10.1364/AO.41.006080

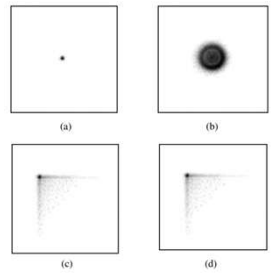
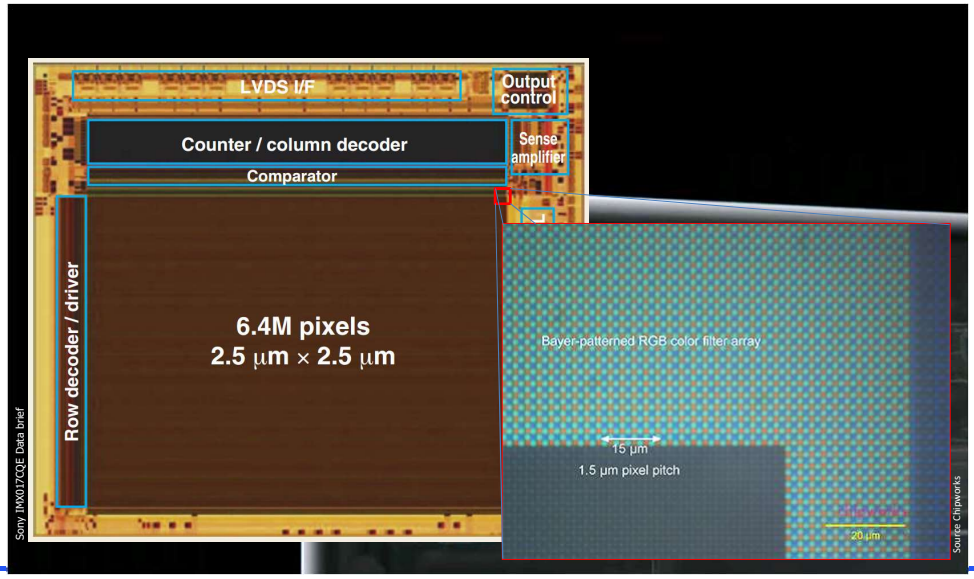


Figure 3. The PSF of the traditional imaging systems (a) in focus and (b) out of focus, and the system with an extended depth of field (c) and (d) for the same focus settings.

Focus on image acquisition: the pixel matrix

CMOS image sensor: a pixel array with circuits on a single chip
System on Chip (SoC)

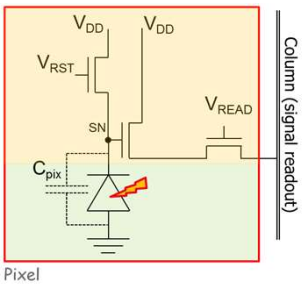


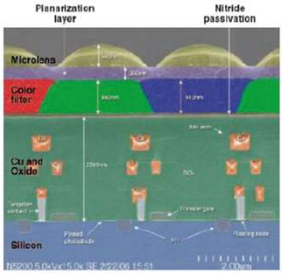
What is a pixel ?

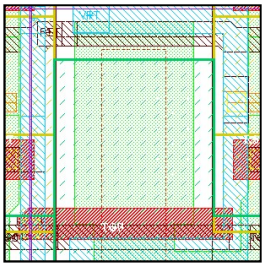
It depends…

on who you are taking to

Various representations of a pixel

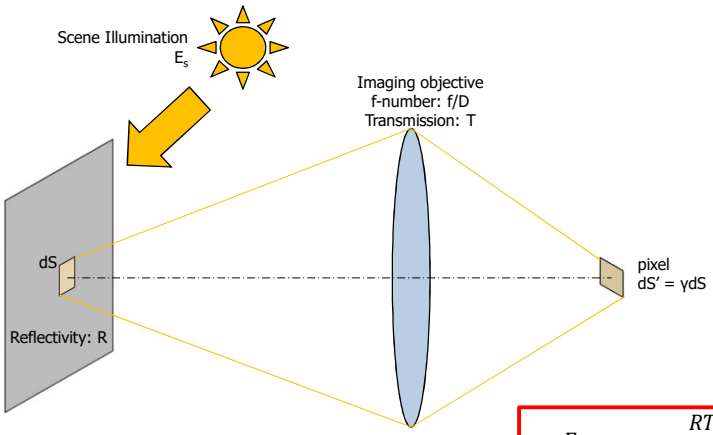






Before let's quantify the amount
on light hitting a pixel

How to calculate the illumination of a pixel?



$$E_p = \frac{RT}{4\left(f/_D\right)^2 (\gamma - 1)^2} E_s$$

Number of photons per pixel

- Main objective with f/D=8 and a transmission of T=90%
- Landscape photography, so $|\gamma| \ll 1$
- Maximum sunlight illumination: E_s=100,000 lux
- Average reflectivity of the scene R=18%
- Pixel pitch 2µm
- Integration time 1/500 s

- $E_p = \frac{RT}{4\left(f/_D\right)^2} E_s \simeq 65\ lux$

- $N_{photons} = E_p \times p_{pixel}^2 \times \tau_{int} \simeq 12500\ photons/pixel$

$1\ lux \simeq 10^{16}\ photons.s^{-1}.m^{-2}$ (sunlight at Earth ground integrated over 400-650nm)

Number of photons per pixel

- Main objective with f/D=4 and a transmission of T=90%
- Landscape photography, so |γ| « 1
- Maximum sunlight illumination: E_s=10,000 lux
- Average reflectivity of the scene R=18%
- Pixel pitch 2µm
- Integration time 1/100 s

- $E_p = \frac{RT}{4\left(f/D\right)^2} E_s \simeq 12\ lux$
- $N_{photons} = E_p \times p_{pixel}^2 \times \tau_{int} \simeq 2500\ photons/pixel$

Number of photons per pixel

- Main objective with f/D=2.8 and a transmission of T=90%
- Landscape photography, so |γ| « 1
- Maximum sunlight illumination: E_s=50 lux
- Average reflectivity of the scene R=18%
- Pixel pitch 2µm
- Integration time 1/30 s

- $E_p = \frac{RT}{4\left(f/D\right)^2} E_s \simeq 0.25\ lux$
- $N_{photons} = E_p \times p_{pixel}^2 \times \tau_{int} \simeq 350\ photons/pixel$

Number of photons per pixel

- Main objective with f/D=16 and a transmission of T=90%
- Macro photography, γ = -1
- Maximum sunlight illumination: E_s=10 000 lux
- Average reflectivity of the scene R=18%
- Pixel pitch 2µm
- Integration time 1/100 s

- $Ep = \frac{RT}{4\left(f/D\right)^2 \times (\gamma-1)^2} E_s \simeq 0.40\ lux$

- $N_{photons} = E_p \times p_{pixel}^2 \times \tau_{int} \simeq 160\ photons/pixel$

Keep in mind for noise part

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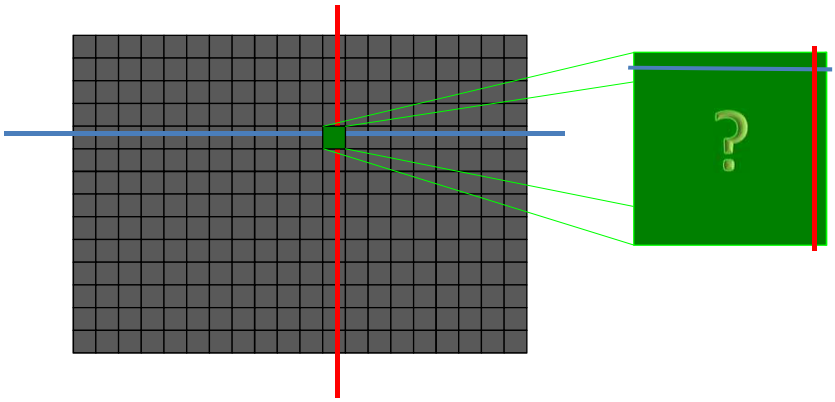
What do we need to make a pixel?



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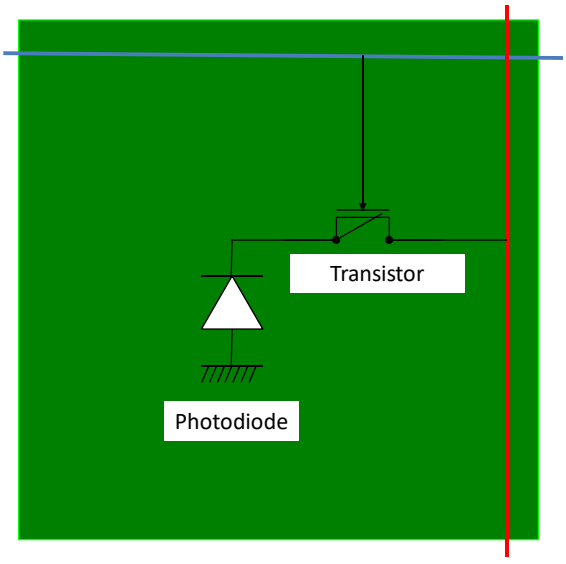

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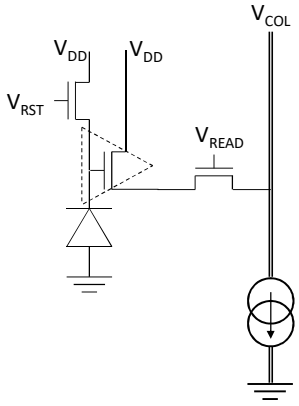
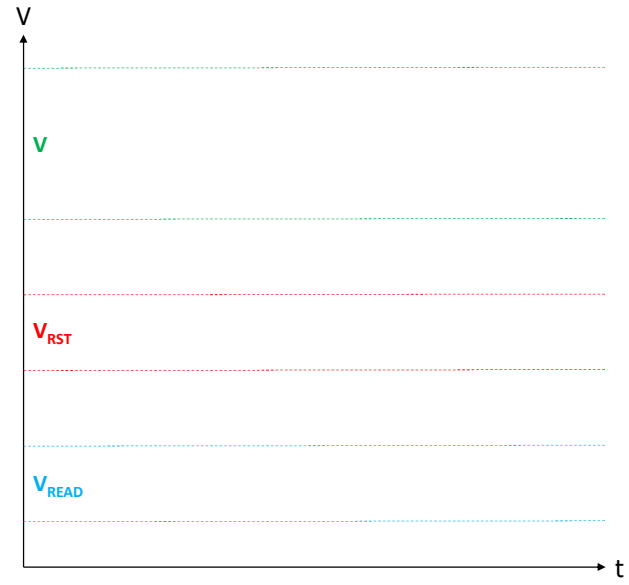
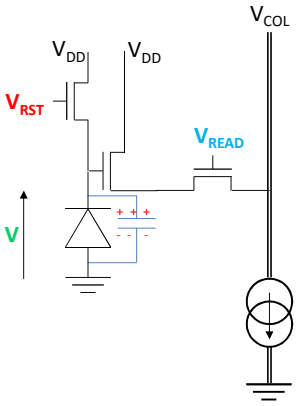
Active Pixel Sensor (APS)

- 3 transistors pixel denoted 3T
  - Photodiode
  - Reset transistor
  - Read (addressing) transistor
  - Source follower transistor

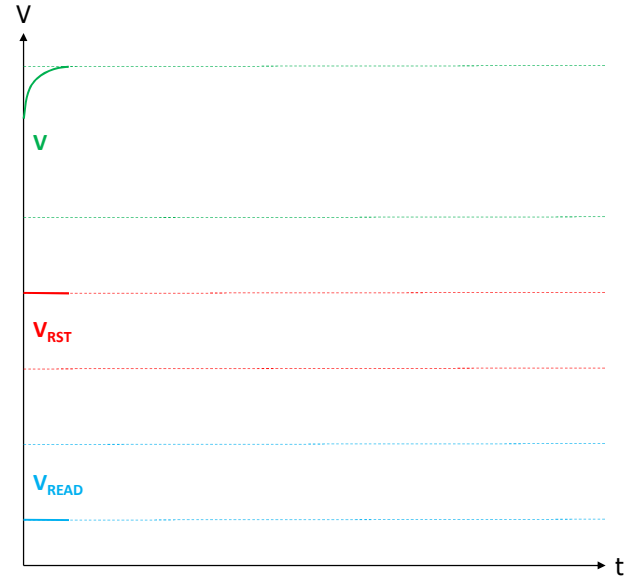


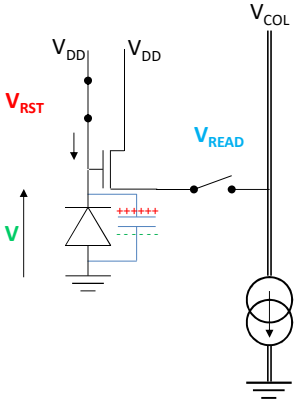
3T pixel timeline





3T pixel timeline





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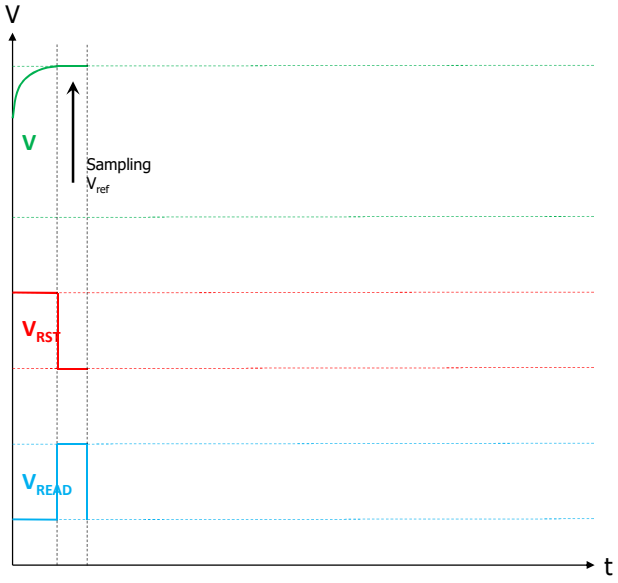

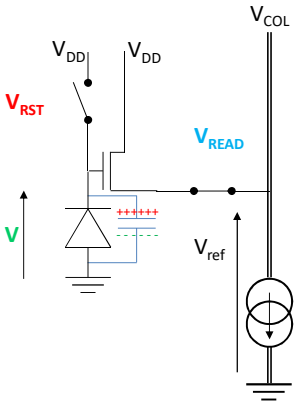

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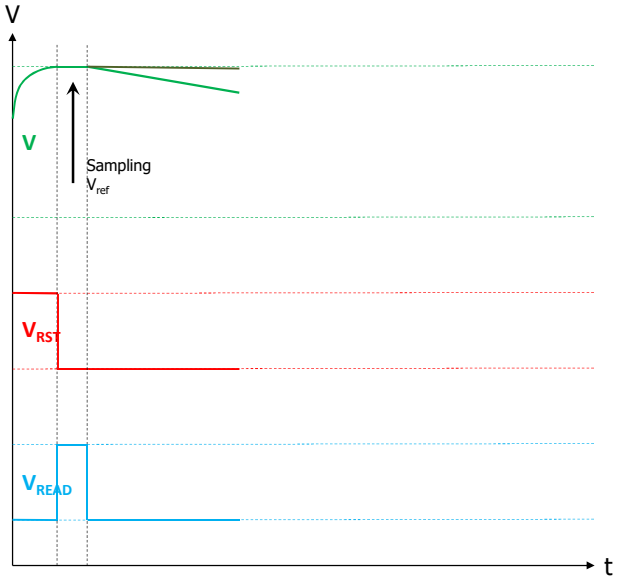

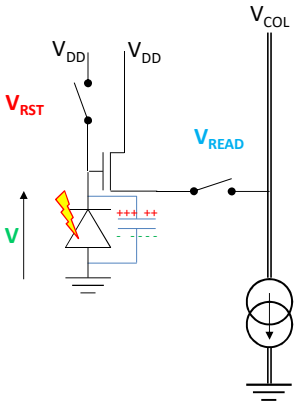

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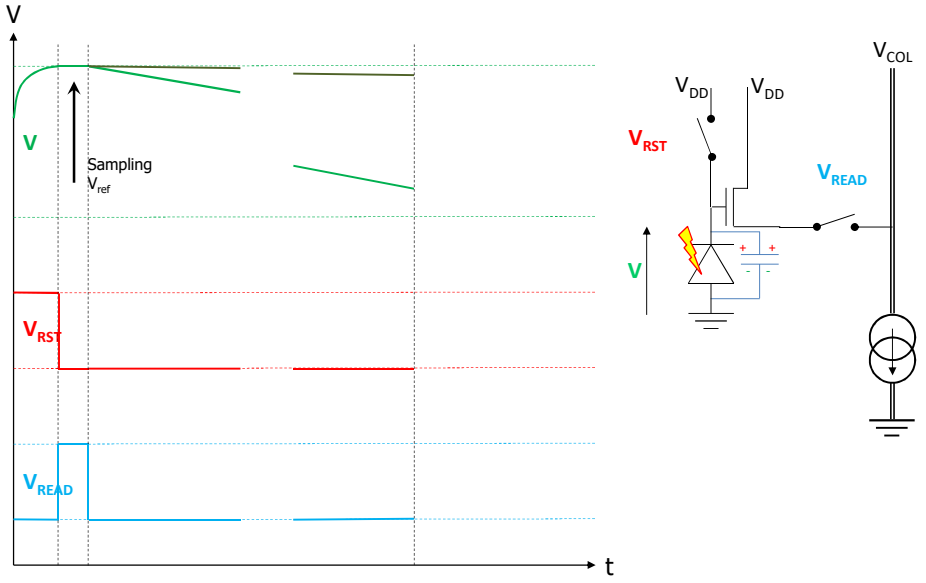

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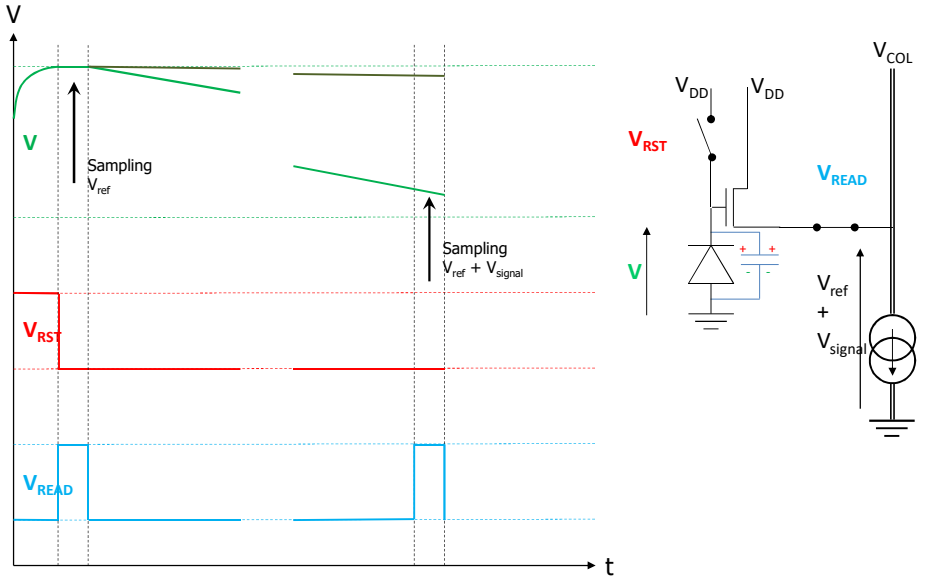

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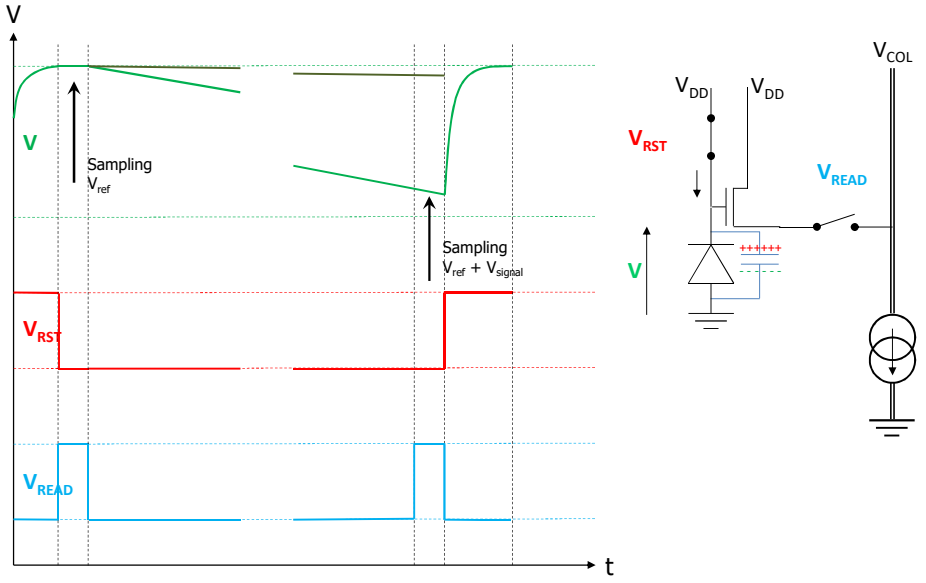

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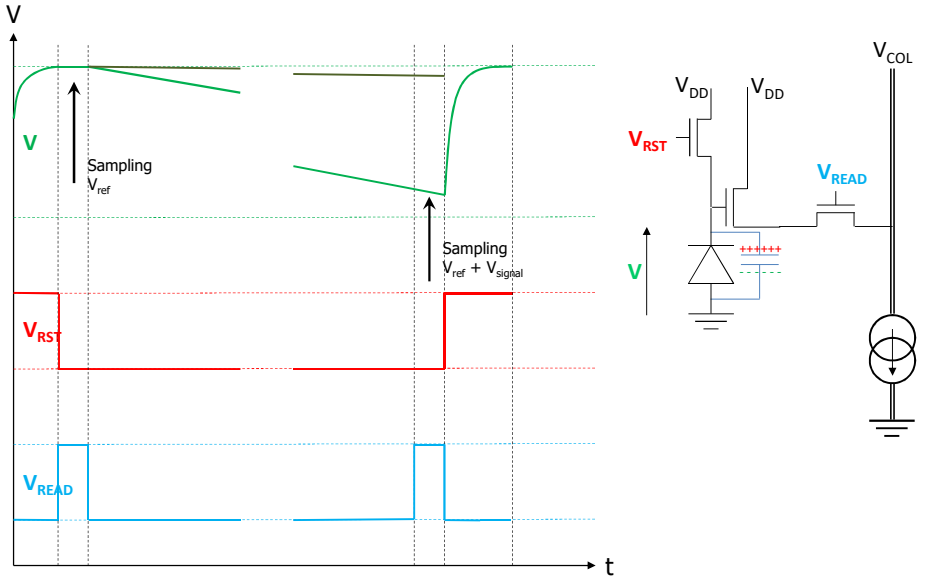

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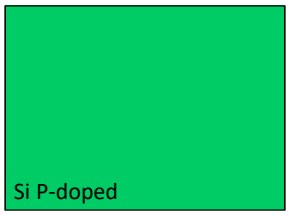
How to do it?

- How to design and process pixel on silicon wafer?
  - How to do a photodiode ?
  - How to do a transistor ?

Process for a photodiode

- PN junction
  - Based on P-doped silicon substrate (e.g. dopant Bore)
  - Local ion implant of N-doping (e.g. Phosphor)



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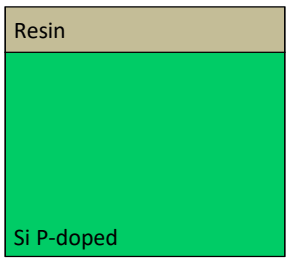

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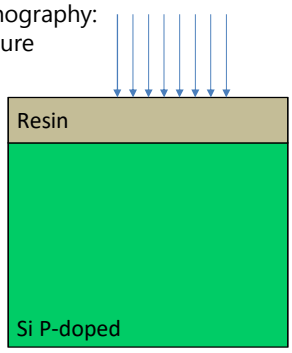
Photolithography:
- Exposure



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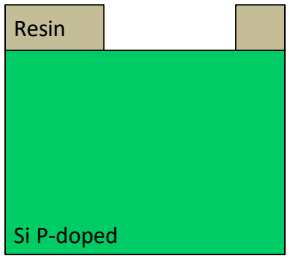
Photolithography:
- Exposure
- Development



Process for a photodiode

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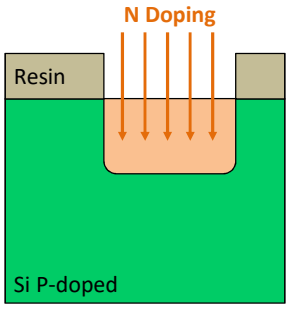
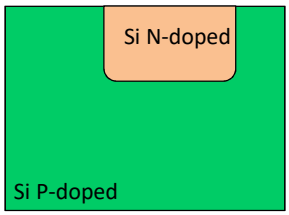
Ion implantation



Process for a photodiode

- PN junction
  - Based on P-doped silicon substrate (e.g. dopant Bore)
  - Local ion implant of N-doping (e.g. Phosphor)

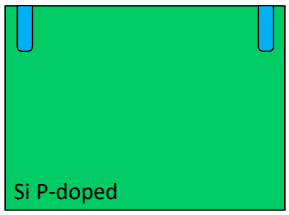
Resin stripping



Process for a transistor

- Source / drain: doped area
- Grid: control potential between S / D

STI (Shallow Trench Isolation) :



Process for a transistor

- Source / drain: doped area
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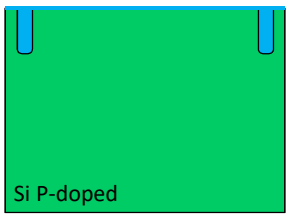
Grid oxide deposition



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- Source / drain: doped area
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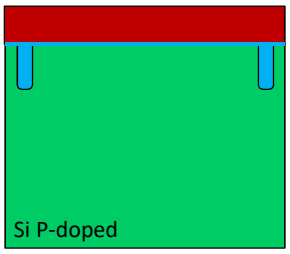
Grid deposition (polycrystalline silicon)



Process for a transistor

- Source / drain: doped area
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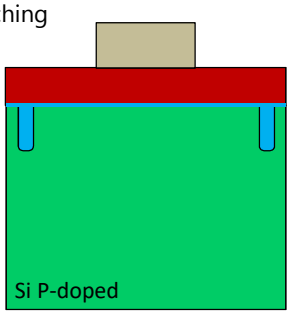
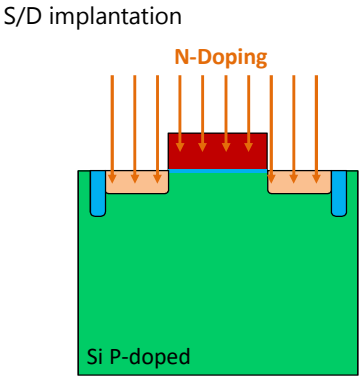
Grid localization
- photolithography
- etching



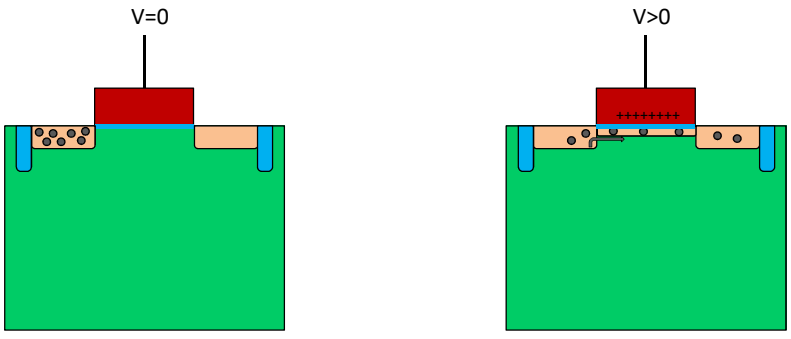
Process for a transistor

- Source / drain: doped area
- Grid: control potential between S / D

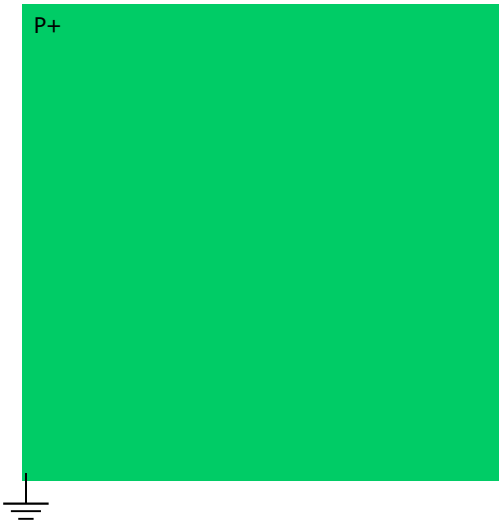


MOSFET transistor

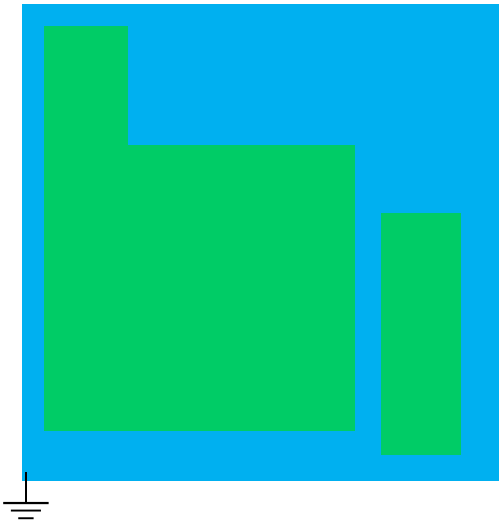
- How does it works



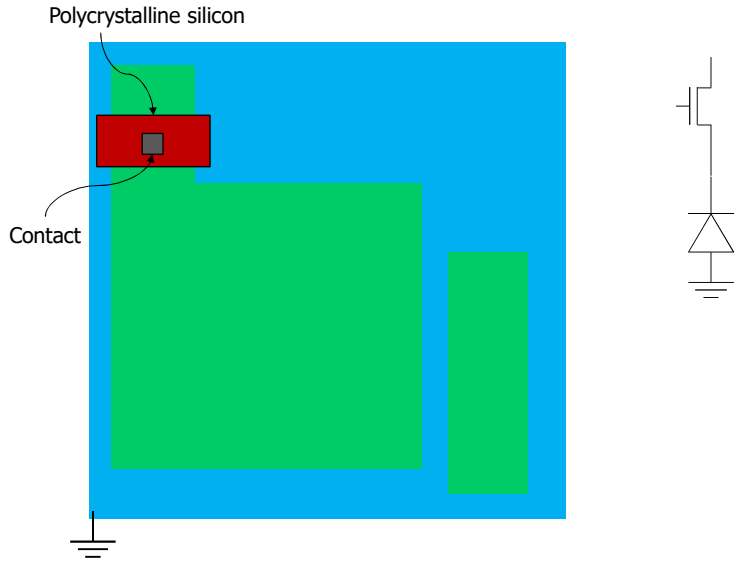
How to draw it? 3T pixel layout



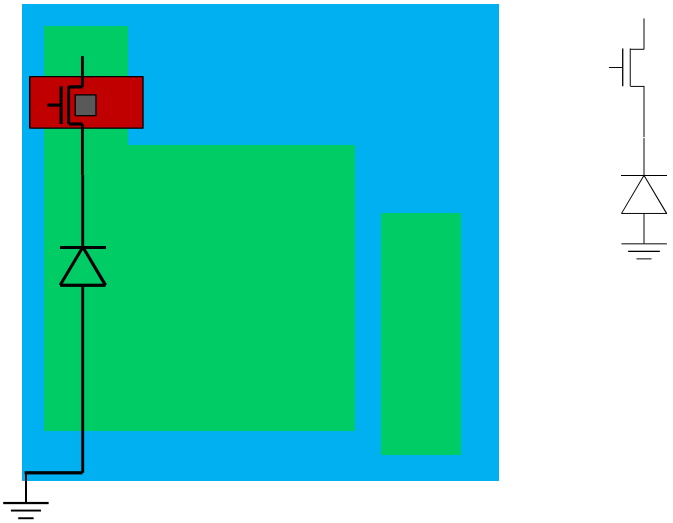
3T pixel layout



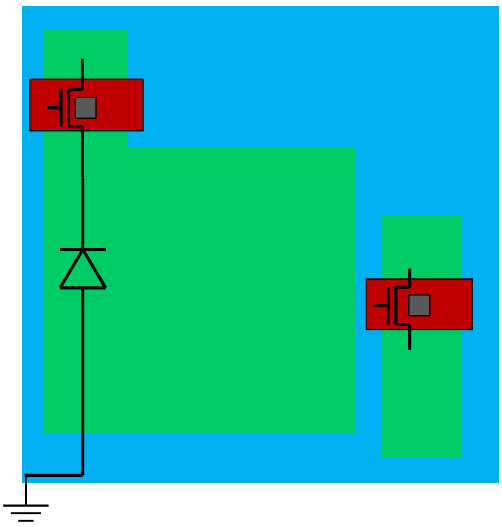
3T pixel layout

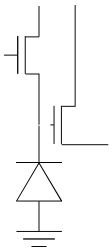


3T pixel layout

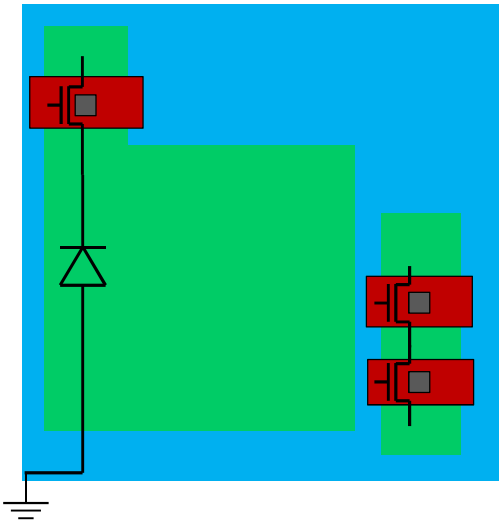


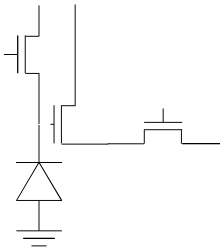
3T pixel layout



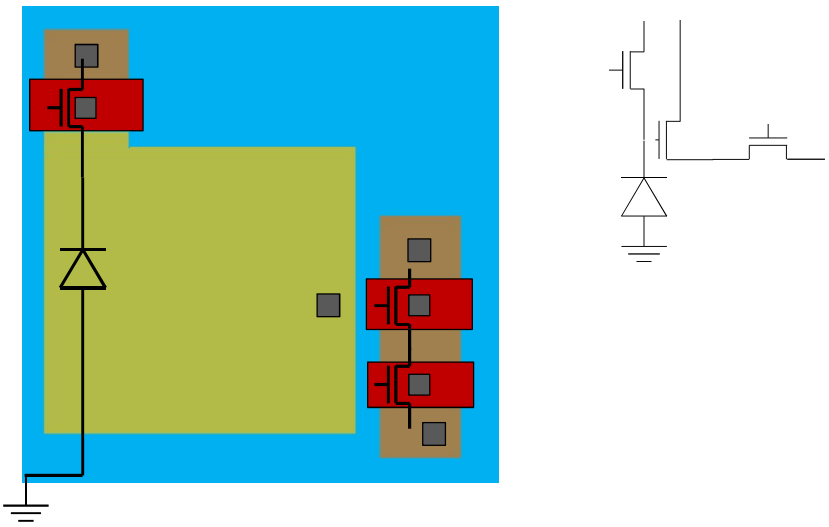


3T pixel layout

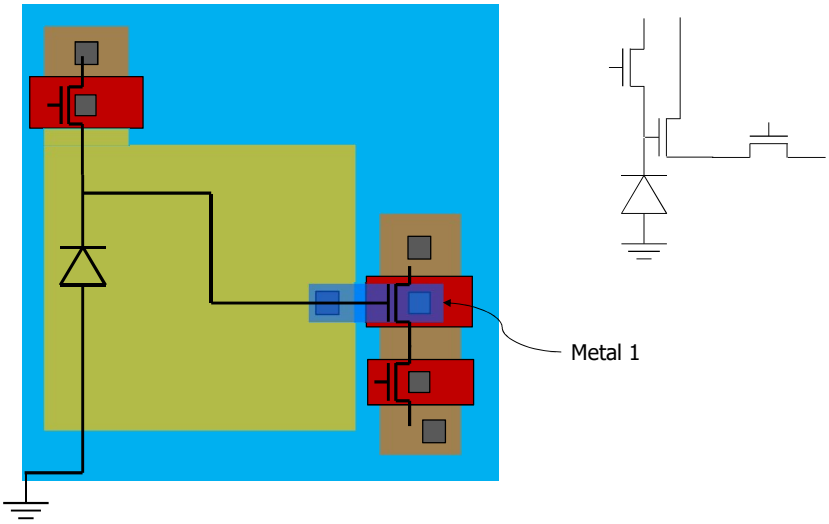




3T pixel layout



3T pixel layout



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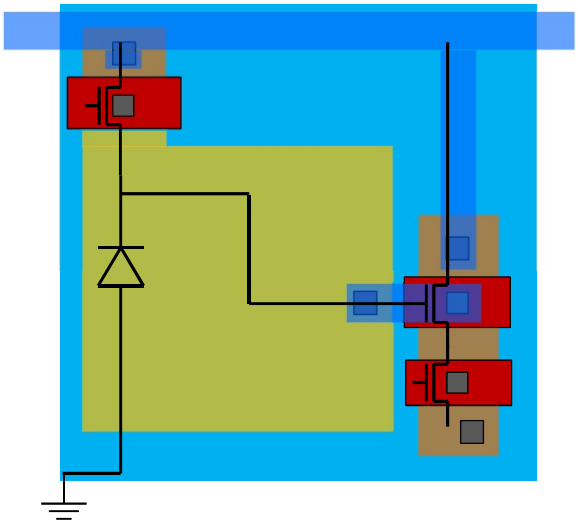
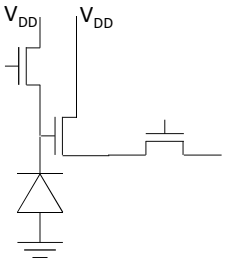
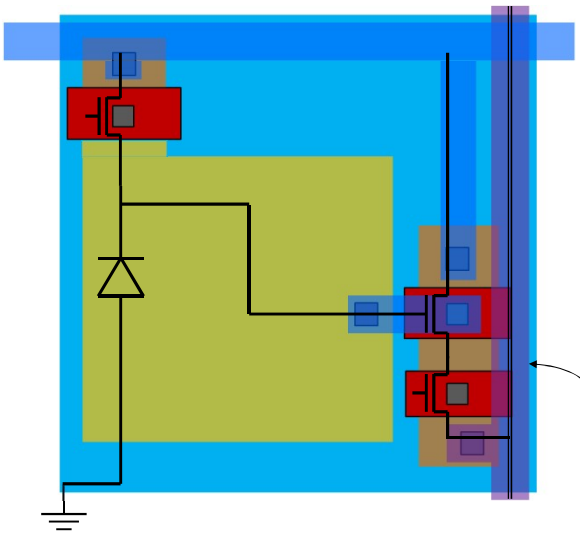
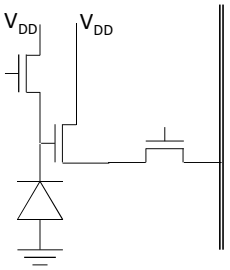




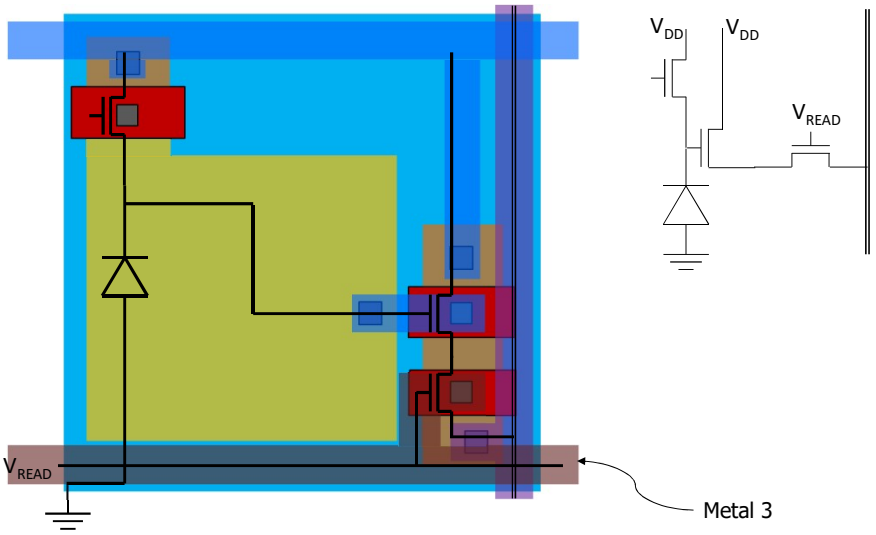
3T pixel layout



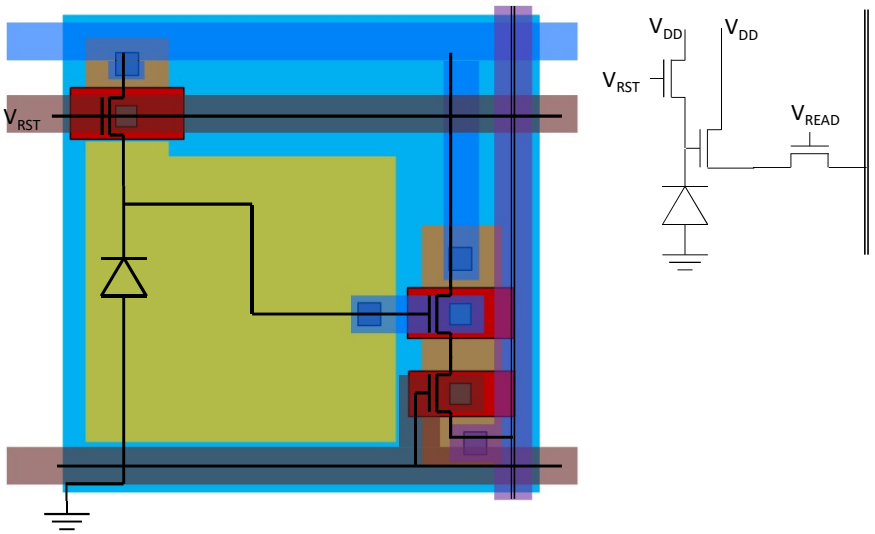


Metal 2

3T pixel layout

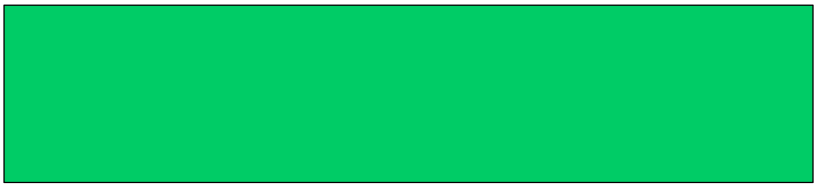


3T pixel layout

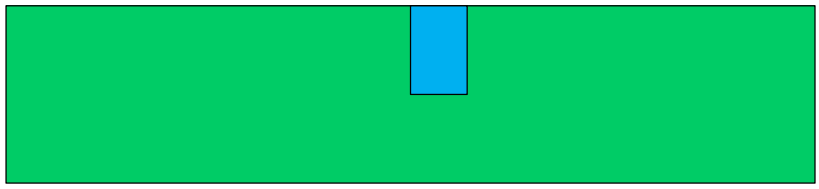


Now, how to process it?

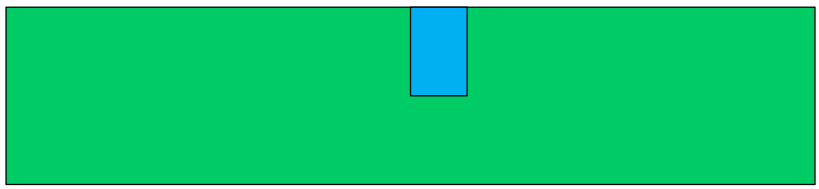
CMOS process



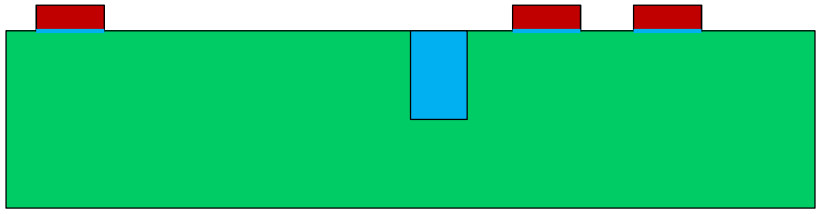
CMOS process



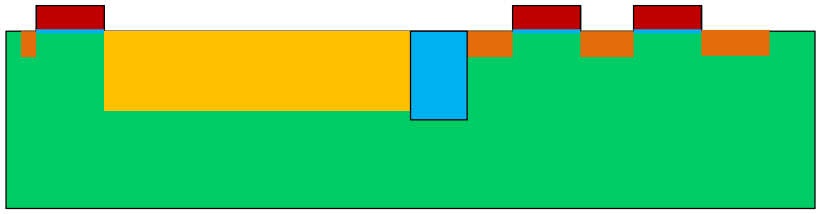
CMOS process



CMOS process



CMOS process



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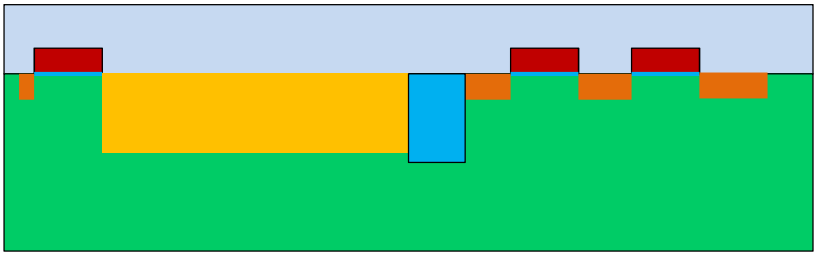

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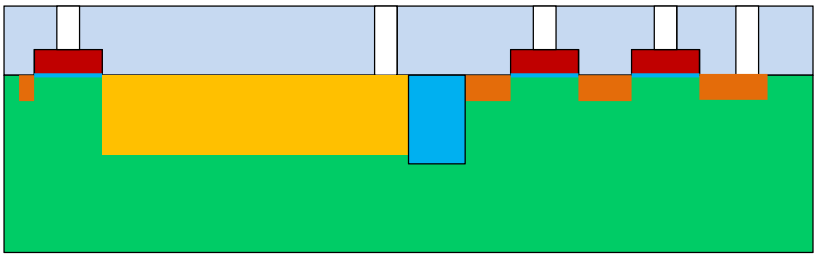

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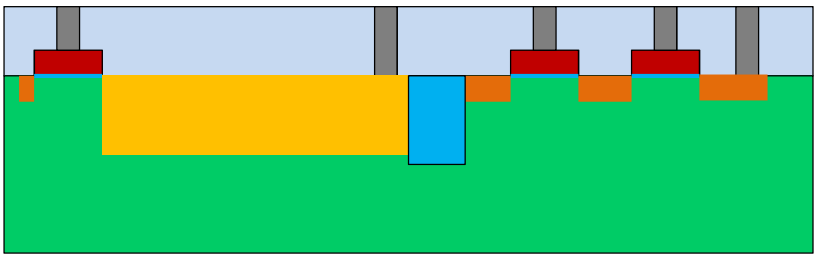

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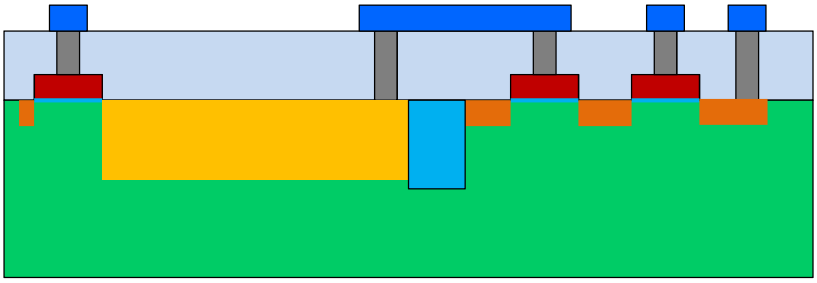

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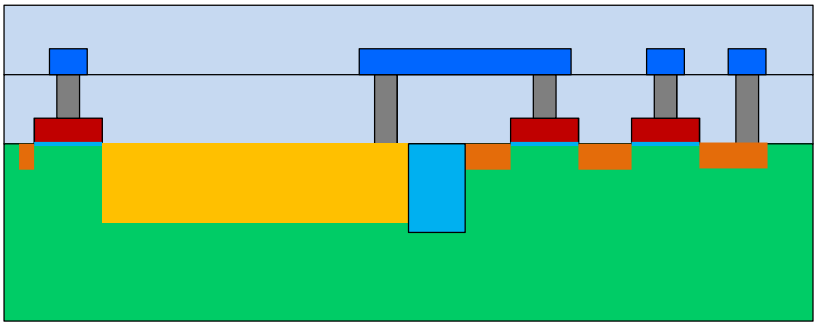

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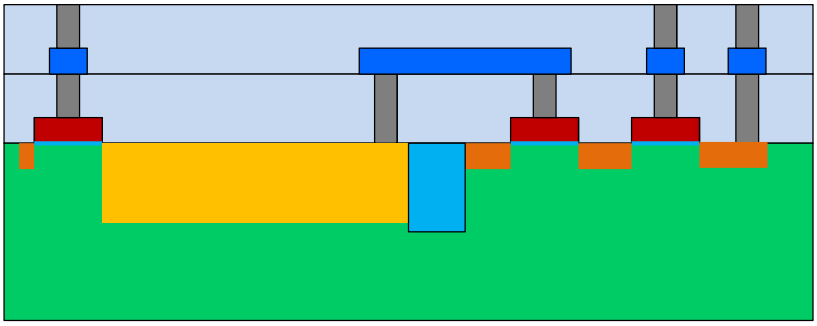

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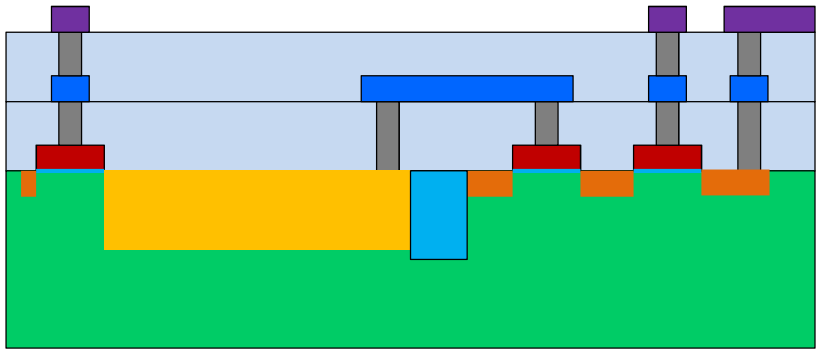

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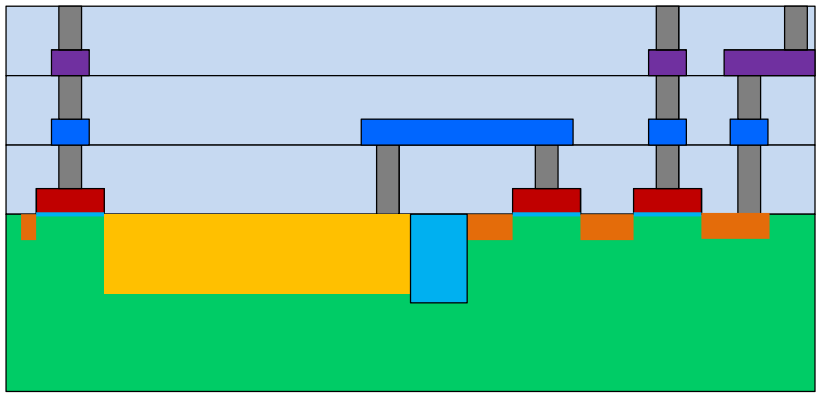

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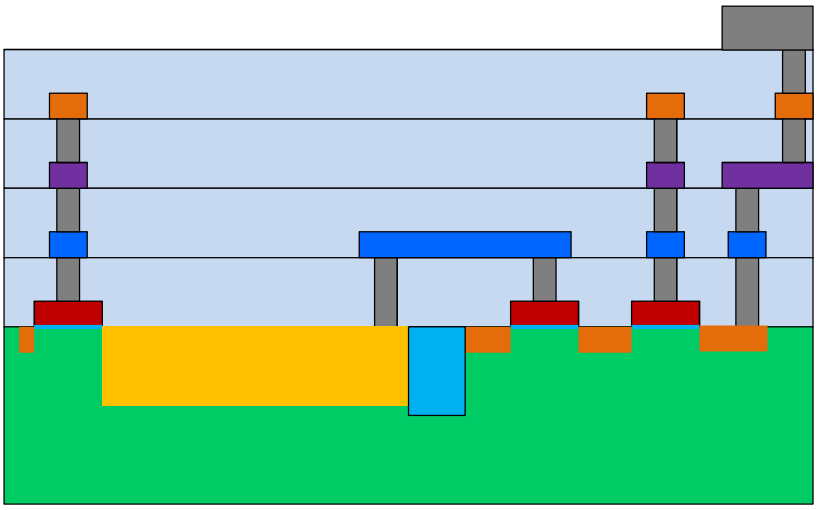

CMOS process