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Implementation of a High Speed Adaptive Modular Pulse Compressor

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RÉSUMÉ

Une architecture efficiente et flexible pour processeurs de correlation a haute vitesse est presentée. Cette architecture est construée a base d'une combinaison de 'overlap discard', 'overlap add' et des techniques de correlation rapide. Le datarate du système est une fonction lineaire de nombre des unités de processeur. Le longueur de filtre augmente lineairement avec le nombre des modules au processeur. Pour un certain configuration de processeur le longueur de reference et le datarate maximum sont interchangeables. La séquence de reference peut être renouvellée chaque novelle séquence de data. On peut trouver des applications dans le domaine de traitement des signaux radar, radar a l'aperture sythetic au temps reel, et la preparation des signaux sonar et images.

ABSTRACT

In this paper, an efficient and flexible architecture is presented for high speed correlation (convolution) processors. The architecture is based on a combination of overlap discard, overlap add and fast correlation techniques. The system datarate increases linearly by adding identical compressor units, while the reference length (filter length) increases linearly with the number of modules in the processor. Given a choosen processor configuration, reference length and maximum datarate are freely exchangeable. The reference sequence can be updated every new data sequence. Applications are, among others, in the field of radar signal processing, real time Synthetic Aperture Radar (SAR), sonar and image processing.

Introduction

Radar pulse compression or 'matched filtering' is basically a cross correlation operation on a replica of the transmitted radar signal and the received echo signal. After a radar transmission at time t=0, the receiver signal is correlated with the replica. A high correlation value at time t_d indicates the presence of a target at a distance $d=c.t_d/2$, where c is the velocity of light. The correlation operation enhances the detection possibilities of a radarsystem.

Conventional radar systems perform the pulse compression operation by using Surface Acoustic Wave (SAW) devices. SAW devices offer high speed (several hundreds of MHz) at relatively low resolution (6-8 bits). Besides, for each unique transmitted waveform a matched set of 2 SAW devices is needed (transmitter and receiver), which forms a logistical drawback. Conventional FIR filter solutions offer higher waveform flexibility and higher resolution (8-16 bits) but low speed (several MHz) and short filter lengths.

This paper presents an architecture and an implementation of a high resolution high speed digital pulse compressor, based on a combination of overlap discard and overlap add techniques using fast correlation. This architecture is capable to handle arbitrary transmit waveforms (references) that may change from pulse to pulse. It can process infinitely long echo data sequences and can incorporate (block) floating point data processing. The architecture exploits a two level modularity, which enables a linear increase in datarate by adding more compression units, and a linear increase of maximum reference sequence length by adding compressor modules. Performance and filter length are freely exchangeable. The approach opens up interesting possibilities for instance in the field of radar signal processing, high resolution real time SAR processing, high speed digital filtering, sonar and image processing.

Sectioned fast correlation

For the purpose of high performance, the correlation values will be calculated using FFTs. Suppose the sequence h(n) represents the replica of the transmitted signal with h(n)=0 for n<0 and n>(Lh-1), where Lh is defined as the length of h(n). Suppose the sequence x(n) represents the received radar echo signal with x(n)=0 for n<0 and n>(Lx-1), where Lx is defined as the length of

x(n). Let $x_p(n)$ and $h_p(n)$ be sequences with a period of L samples, where L=Lh+Lx-1, $x_p(n)=x(n)$ for $0\leq n\leq(Lx-1)$, $x_p(n)=0$ for $Lx\leq n\leq(L-1)$, $h_p(n)=h(n)$ for $0\leq n\leq(Lh-1)$ and $h_p(n)=0$ for $Lh\leq n\leq(L-1)$. Then the correlation function $R_{hx}(k) = DFT\{r_{hx}(n)\}$ is given by $R_{hx}(k)=X(k).H^*(k)$ where $X(k)=DFT\{x(n)\}$ and $H(k)=DFT\{h(n)\}$ are given by (1) and (2).

$$H(k)=\sum_{s=0}^{L-1} h_p(s).\exp(-j.2\pi.s.k/L) \qquad (1)$$

$$X(k)=\sum_{s=0}^{L-1} x_p(s).\exp(-j.2\pi.s.k/L) \qquad (2)$$

where k=0,1,2,...

Because practical FFT processors (DSPs) have a limited transform length L_{fft}, long x- and h-sequences have to be divided into sections. Here, for the x- and h-sections we choose a length of L_{fft} samples and Nh samples, respectively, and

$x_i(n)$	: i^{th} section of x(n); i=0,1,2,...
$h_j(n)$	: j^{th} section of h(n); j=0,1,...M-1
Nh=Lh/M	: section length of $h_j(n)$
M	: number of h-sections $h_j(n)$

The overlap between adjacent x-sections $x_i(n)$ is (Nh-1) samples. Subsequent h-sections are non-overlapping. Let:

$r_j(n)$	: partial correlation of $h_j(n)$ and x(n)
$r_{ji}(n)$	: partial correlation of $h_j(n)$ and $x_i(n)$
$r_{j(i+1)}(n)$	: partial correlation of $h_j(n)$ and $x_{i+1}(n)$

Due to wrap around, caused by the Fourier transform, the last (Nh-1) samples of $r_{ji}(n)$ will be discarded and replaced by (Nh-1) corresponding samples of the next partial result $r_{j(i+1)}(n)$.

Each $r_{ji}(n)$ contributes L_{fft}-(Nh-1) 'body samples' to $r_j(n)$.

Fig. 1 gives an example (Nh=3, L_{fft}=5, Lx>>L_{fft}).

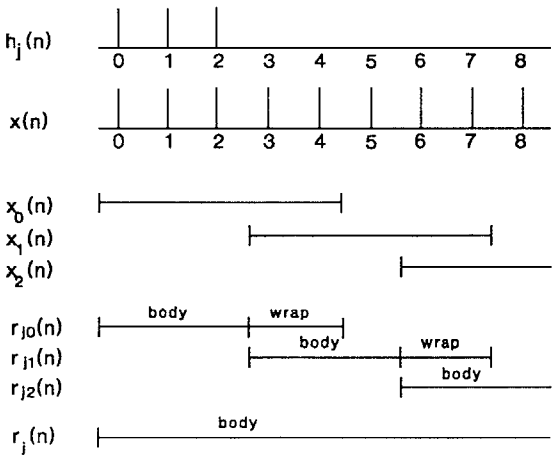

Fig.1: overlap discard correlation using DFT/FFT (Nh=2,L_{fft}=5)

When sectioning h(n), the overlap add method is used to combine the M partial correlation results $r_j(n)$ into the total correlation r(n).

Architecture

The given correlation method can be translated into a processor architecture that offers large flexibility for changing reference sequences, and the possibility to increase performance by just adding identical modules/units (fig. 2). For this purpose, it exploits a two level modularity. In fig. 2, the block SCALE & ADD has a delay of D sample periods, which is compensated by corresponding delays in the x- and h-buses between subsequent modules.

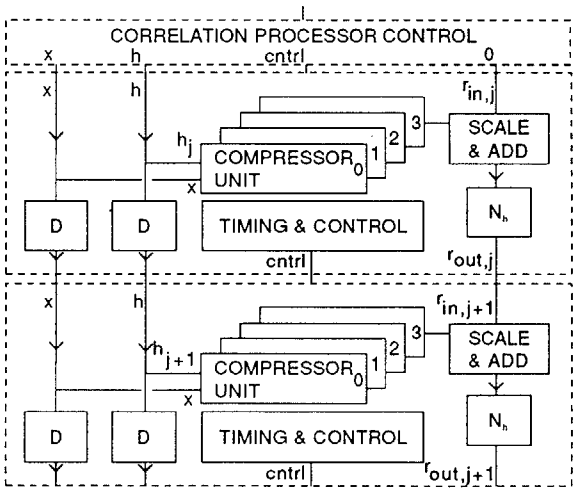

Fig.2: system architecture (M=2,P=4)

Module level

This first level of modularity in fig. 2 enables the sectioning of h(n) over M modules. Each module handles Nh reference samples. At the start of a correlation operation, the processor control block simultaneously puts the sequences x(n) and h(n) onto the x-bus and h-bus, respectively. Subsequently, each module takes its own section $h_j(n)$ from the h-bus and simultaneously starts the input of x-data. Thus module j+1 starts the correlation operation Nh samples after the start of module j, and therefore automatically skips the first j.Nh samples of x(n). Consequently, the output $r_j(n)$ of module j must effectively be delayed with Nh sampleperiods with respect to $r_{j+1}(n)$, prior to the overlap add addition in the $j+1^{th}$ module (fig. 2). The sequence $r_{out,j+1}(n)$ consists of the summation of $r_{j+1}(n)$ and $r_{out,j}(n)$.
Programming of the modules (mode,Nh) can be done by distributing the programming data through the x-bus or h-bus prior to the start of the correlation operation. The scaling function in the blocks SCALE & ADD is needed when (block) floating data must be applied to the adder.

Compressor Unit level

Inside each correlation module, P Compressor Units perform the actual fast correlation operation using high performance FFT processors. The basic architecture of the Compressor Unit is given in fig. 3.

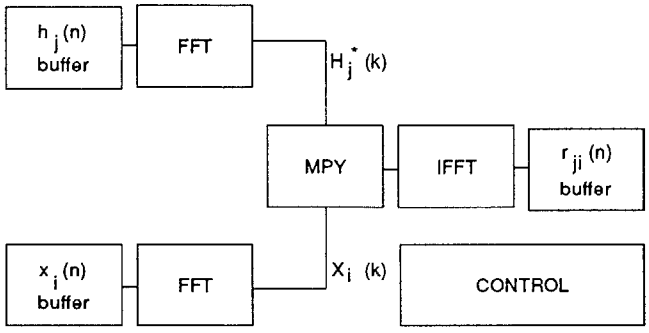

Fig.3: Compressor Unit architecture

The buffers at the inputs and the output enable the Compressor Unit to run at maximum internal speed, independent of the system datarate Dr. This has a positive effect on the 'busy time' and the number of Compressor Units needed. In each module of fig. 2, the four Compressor Units are circularly activated when processing long echo sequences x(n). The input of x-sections by subsequent Compressor Units as well as the output of the resulting sequences $r_{ji}(n)$ is following the discussed overlap discard method. At the start of each new echo sequence, a new reference sequence can be applied at the same time. At a constant value of Nh, new data sequences can be applied immediately after the previous sequence.

In the processor architecture, the control functions are locally implemented which is illustrated, among others, by the circular activation of the Compressor Units within a module. The control of this approach is performed by the Compressor Unit itself. This has a strongly benificial influence on the complexity of the module control.
Side lobe cancellation, as is often used in radar systems, can easily be performed by applying a weighting function on h(n) in time domain.

Performance

Let Tfft be the transform time of the (I)FFT processor at transformation length L_{fft}, and Nh_{max} the maximum number of reference samples per module. Then the number of Compressor Units P needed for continuous correlation processing (infinitely long echo sequence x) is given by

$$P = Dr.Tfft/[L_{fft}-(Nh_{max}-1)] \qquad (3)$$

From (3) it is obvious that a larger FFT length, as well as a lower value of Nh_{max}, results in a more compact processor configuration. The total number of Compressor Units in the total correlation processor is M.P, where $Lh_{max}=M.Nh_{max}$
It can be shown that, given L_{fft}, for values of Nh larger than Nh_{opt}, the total number of Compressor Units (M.P) can be reduced by adding an extra module. Given Lhmax, this results in a lower value for Nh_{max}, and subsequently in fewer Compressor Units (P) per module.
In the case of processing short sequences (order L_{fft}), due to the block processing character the availibality aspect of the Compressor Units must be taken into account. This can result in one or more extra Compressor Units per module and/or the necessity to obey a time interval between subsequent x-sequences.
Important aspect of the correlation processor as indicated by (3) is that the maximum datarate Dr_{max} increases linearly with the number of Compressor Units P per module, and is in practice mainly limited by the speed of local memory and bus interconnect. Also, within the constraint of a given number of Compressor Units P, the

datarate Dr_{max} and the reference length Nh can be freely exchanged.
When using (block) floating point FFT processing DSPs and high system datarates, additional care has to be taken for the 'on the fly' scaling of the module output data prior to the overlap add operation.

Prototype

TNO-FEL has successfully implemented a prototye correlation processor with a M=1, P=2 configuration. A photograph of the prototype Compressor Unit is shown in fig. 4. The final version of the full Compressor Unit will be available 1993/Q4 and will be implemented on 1 E-6 board. This board will be controlled by an Application Specific Integrated Circuit (ASIC) that is currently under development at TNO-FEL. The Compressor Unit offers a system datarate of Dr_{max}=40 MHz, a reference length of Nh_{max}=1020 samples and has a processing power of 375 MIPS (multiplications, i/o time incorporated). Both sequences x(n) and h(n) are applied via complex input data buses that are 2x16 bits wide. The complex output data is also 2x16 bits and is accompanied with a 6 bit block floating point exponent.

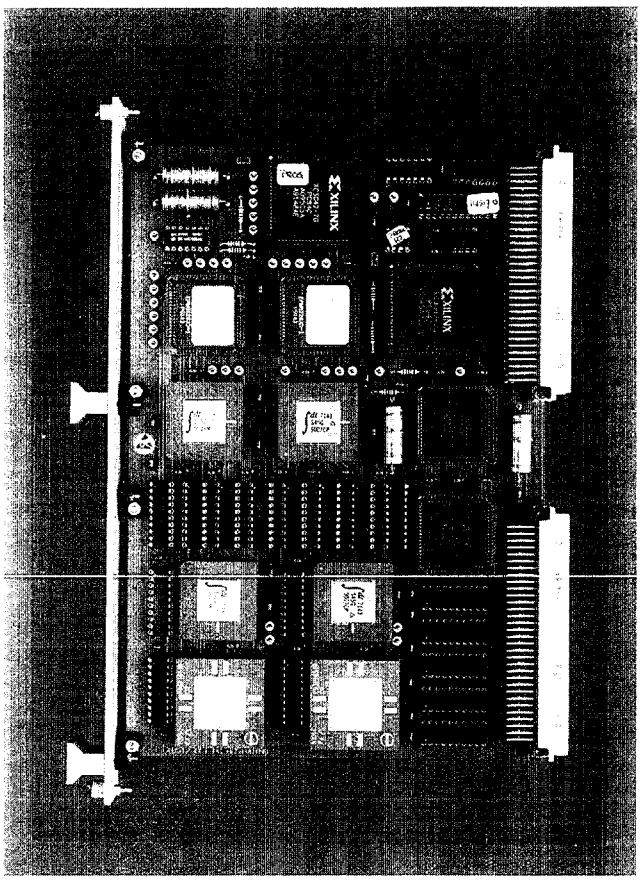

Fig.4: prototype implementation of Compressor Unit

Conclusion

The discussed architecture of the correlation processor combines high datarates with relatively long reference lengths (filter lengths) and a large flexibility with regards to changing filter characteristics. It enables the composition of high performance correlation processors which the configuration can be tuned to customer requirements. By adding more complex units/modules virtually any performance requirement can be met, only limited by the speed of memory and interconnect. The given architecture is easily adaptable for high speed convolution purposes. The use of high resolution DSP components expands the radar application area to, for instance, high resolution real time SAR processing, sonar, image processing (for example, pattern recognition) and production monitoring.