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BIT SYNCHRONIZERS - THE STATE OF ART

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RESUME

On expose ici l'état de l'art des diverses méthodes utilisées pour construire un synchronisateur de bits.

J'ai partagé les méthodes en deux, la première méthode est basée sur les techniques de l'éstimation optimales, et la deuxième méthode est basée sur un traitement nonlinéaire du signal MIC.

Pour chaque methode des deux on présente le schéma fonctionel, les principales performances et les devirses techniques d'implementations.

L'article est terminé avec un ensemble de 33 références, et peut être considéré comme un guide tres util pour les ingineurs qui travaillent dans le domain de la synchronisation de bits.

SUMMARY

This review paper presents the state-of-art of different building methods of self bit synchronizers (BS) for PCM signals. Two basic methods are used to build self BS. The first method is based on optimum estimation techniques and the second method is based on nonlinear processing of the PCM.

The paper presents the basic functional blocks, the main performance parameters and the possible implementation techniques related to each method.

The paper is terminated with a set of 33 refrences and can be considered as a useful guide to the engineers working in the field of bit synchronization.

BIT SYNCHRONIZERS- THE STATE OF ART

I-INTRODUCTION

In general binary communication system such as a pulse-coded modulation(PCM)system, the signal alphabets normally contain two levels,i.e.,"1" or "0". The reception task involves the problem of establishing an optimal decision rule for distinguishing between these two signal levels. Unfortunately, the optimal decision rules depond not only on the formats of the received signal,but also on the characteristics of all the disturbances occuring during the transmission. The well-known optimal receiver in a Bayes sense such as the correlation detector or matched filter has been used to handle the situation in which the incoming signal consists of precisely known binary signals and additive white Gaussian noise [1]. However, a perfect synchronization of the received signal with respect to a local clock is usually necessary in such a scheme befor bit-by-bit optimal detection can be performed. The subsystem which delivers the localclock at the receiver side is called bit synchronizer (BS)(In French the word"synchronisateur primaire" usually means the combination of bit synchronizer and data detector [2]) . The process of generating the local clock is called "bit synchronization".

Previous methods of establishing bit synchronization consists of transmitting a pilot signal is used at the receiver side to derive a phase-locked loop (PLL) tuned to a frequency numeriqually equal to the bit rate F. The design of the BS in this case turns to be a design of a PLL. The theory of analoge PLL is well established and the designer can be refered to Blanchard [3] and Gardner [4] . On the other hand, the digital phase-locked loops (DPLL) constructions are not unique and generally their design is not an easy task. Several configurations of DPLL are reviewed by S.C Gupta [5].

Estblishing bit synchronization using transmitted pilot signal is not efficient, since the pilot signal consumes both power and bandwidth.

A more desirable svstem of synchroniz tion uses the received data itself to de ive the local clock. The BS in this case is called data derived BS or self BS. The signal at the input of self BS is given by:

$$x(t) = s(t) + n(t).$$

with

$$s(t) = \sum_{k=o}^{\infty} a_k \; q(t-kT-\Delta t), \text{ the PCM signal} \qquad \text{Eq (1)}$$

a_k is the polarity ($\pm$ 1) of the k^{th} bit (assuming bipolar signaling), T is the duration of the received bit($T = \frac{1}{F}$, F is the bit rate) and Δt is the inital time shift between the locally generated clock and the instants of transition of the PCM signal. The signal form q( ) is related to the code type (For example NRZ,Biphase,RZ,..) and the communication channel characteristics. n(t) is additive noise at the BS input.

The problem of establishing bit synchronization in its general form. is to find the values of T and Δt. This problem can be viewed in two ways:

(1) first, to be considered as parameter estimation,problem, where the parameters to be estimated are T and Δt. The constructions of BS based on estimation. techniques will be reviewed is sectionII.

(2) Second, as problem of generating a spectral line component corresponding to the bit rate F by nonlinear processing of the received data signal.The constructions of BS based on nonlinear processing will be reviewed in section III

The performance of a particular BS is generally measured by the following parameters [6]:

(a) Acquisition time (T_{acq}):the time interval measured between the instant when the noisy PCM signal(x(t))is applied at the input of BS and the instant when the clock signal is regenerated with small (predetirmened) synchronization error.

(b) Synchronization error(λ) given by the ratio $\Delta t/T$

where $\widehat{\Delta t}$ is the estimated value of Δt, the effect of λ on the error probability in the matched filter is given in [11] .

(c) Value of threshold: difined as the value of E/N_o (E being the energy of one bit and N_o is the one sided power spectral density of the noise) at the input of BS below which the clock signal is not useful.

II- BS BASED ON ESTIMATION TECHNIQUES

The decision and estimation techniques find many applications in signal processing, especially demodulation and synchronization [7-9] .

The estimation technique which is well known in the field of bit dynchronization is the Maximum A postriori Probability(MAP) estimation technique [10, 11]. It is assumed that the bit duration is constant and known at the receiver side, the inital time shift Δt is constant(but unknown) during an observation interval MT,M is an integer, the noise n(t) is white Gaussion zero mean noise, and the bits "0" and "1" are equiprobable.

There is then only one parameter to be estimated, namely Δt. The optimum value of Δt in MAP sense is that value which corresponds to the maximum of P ($\Delta t/x(t)$), the conditional probability of Δt given x(t). It is shown that [10,11]the optimum value of Δt , is that value which maximizes the following function:

$$f(\Delta t_j, x(t)) = \sum_{k=0}^{M-1} \ell_n \cosh \left(\frac{2}{N_o} \int_{T_j} x(t) q(t, \Delta t_j)\, dt \right) \quad E_q(2)$$

with : $q(t, t_j) = q(t - kT - \Delta t_j)$,

$t_j = jT/N$; $j = 0, 1, 2, \ldots, N-1$

T_j is the interval of integration from $\Delta t_j + (k-1)T$ to $\Delta t_j + kT$

N_o is the one sided power spectral density of the noise n(t)

Cosh ( ) and ℓ_n ( ) are the hyperbolic cosine and the natural logarithms respectively.

Fig(1) shows the practical interpretation of the aboue result . The received signal is crosscorrelated with a stored replica $q(t,t_j)$ in each subinterval , then the log hyperbolic cosine of this result is occumulated over all M subintervals.

The complete bit synchronizer consists of N chains of Fig 1 the value of Δt_j that yields the largest accumulated value is then declared the best estimate $\widehat{\Delta t}$

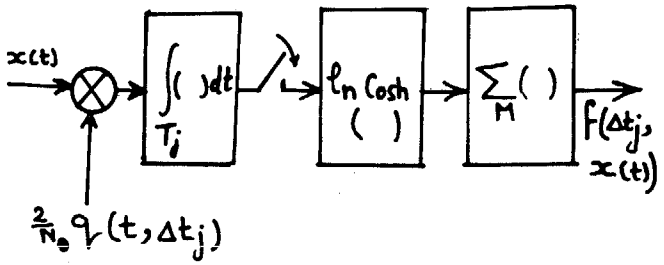

Fig.1. ONE CHAIN OF THE MAP BS

The MAP BS is too complex especially when high accuracy of bit timing is required. Despite its complexity, the performance of the MAP BS is worth studying since it may be used as a standard against which the performance of easier to implement synchronizer configurations may be judged.

Luecke and wintz [12]evalute the performance of MAP BS in terms of E ($|\lambda|$), for $\Delta t=o$ Results are given for different pulse shapes q(t), observation interval M, and the signal - to-noise ratio E/N_o.

Several BS configurations motivated by the MAP estimation approach are given by Lindsey [11] . closed loop synchronizers, which enable continuous estimation of Δt when it varies slowly with time, are derived by differentiating Eq(2) with respect to Δt_j(Δt_j is now considered to be continuous variable) and equating to zero. The value $\partial f(\Delta t_j, x(t)) / \partial \Delta t_j$ is used as an error signal applied to the input of a voltage controlled oscillator (VCO) that delivers the clock signal. A simplified block diagram of the closed loop subeptimum BS is shown in Fig.2. The nonlinear phase detector calculates the derivative of $f(\Delta t_j, x(t))$ the loop filter characteristics determines the value of M.

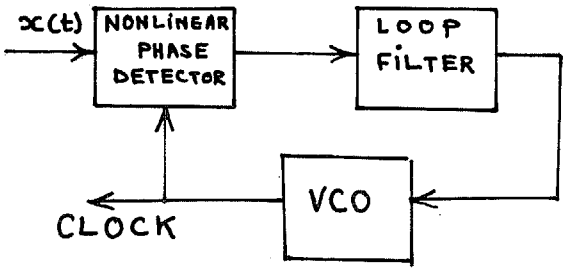

Fig 2. Closed loop BS

The configuration of Fig 2. is a phase-locked loop (PLL) with nonlinear phase detector characteristic. The well known Data Transition Teacking Loop(DTTL) belongs to the configuration of Fig 2. DTTL firstly introduced, intutively, by Lindsey and al [13] in 1968. In 1971, Mengali [14] showed that the DTTL is a suboptimum implementation of the obtimum MAP BS. Cessna et al [15] and Ranson et al [16] propose closed loop BS which are similar to the DTTL.

Performance of DTTL in terms of the variance of the Synchronization error is given in [11] and [17] . Analysis of the DTTL; in correlated Gaussian noise is given by Gangopadhyay et al [18] . It is shown that the performance is improved in this case The DTTL performs well in tracking mode and in low E/N_o (threshold in the order of - 7 dB) and thus applied in coded data transmission.

The mean acquistion time of the DTTL is measured [19,20] and is shown to be relatively long(In the order of 10^5 bit duration)

The Early late Gate(ELG) Bs belongs also to the configuration of Fig 2. Its synchization error is calculated in [4-chap 11] The ELG BS is used in board of satellite in ARGOS system, a system of localation and data collection cooperated between CNES (France) and NASA(USA) [21] .

Nonlinear Estimation technique, using state space representation is used by Hirschler and Peronnet [22] for building BS. The nonlinear estimator, in this case, is an extended kalman filter [9] which delivers an estimate of both Δt and a_k of eq(1). The estimated values are optimal in the least mean square of the error sense. The algorithm derived is recursive and can be implemented using microprocessors. Chow et al [23 , 24] propose another algorithm for estimating both Δt and a_k of eq(1) using linear estimation technique. The application of linear estimation technique is made possible by a pre-correlation operation. It seems that the algorithm of chow et al is more simpler that of Hirchler et al.

II. BS BASED ON NONLINEAR PROCSSING

Consider a binary PCM signal s(t) with symbols $s_1(t)$ and $s_2(t)$. The nespective probabilities of occurance of $s_1(t)$ and $s_2(t)$ are p_1 and p_2. It can be shown [11- chapter 1] that the power spectral density of s(t) is given by:

$$\Phi_S(f) = \frac{1}{T^2} \sum_{n=-\infty}^{\infty} \left| P_1 \quad S_1(nF) + P_2 \, S_2 \, (nF) \right|^2 \delta(f - nF) + \frac{1}{T} \; P_1 \, P_2 \left| S_1(f) - S_2(f) \right|^2 \quad \text{Eq(3)}$$

where

T is the bit duration

F is the bit rate(F=1/T)

$S_1(f)$ and $S_2(f)$ are the Fourier transforms of $s_1(t)$ and $s_2(t)$ respectively.

The first term in the righ hand side of eq(3) represents the line spectral components, while the second term represents the contunous spectral.

Nonlinear processing transforms the PCM signal that contains zero line spectral components into another PCM signal that contains nonzero line spectral components.

The general block diagram of BS based on nonlinear processing is shown in Fig.3.

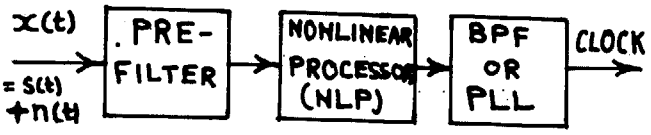

Fig.3.
General Block Diagram of BS. Based on Nonlinear Processing

a) Prefilter

The prefilter transforms the signal waveform into another one suitable for efficient line spectral generation. The prefilter design problem is equivelent to optimum choise of signal waveform at the NLP input.

The prefilter optimum transfer function depends on the PCM code type (NRZ, Biphase,...), on the signal-to-noise ratio at its input and on the type of used NLP. Theoritical results concerning prefilter optimum transfer function are given by Franks et al [26] and Gagliardi [27]. The NLP is assumed to be of square-low type and the PCM signal is NRZ coded. Their critira of optimality is the cancellation of the continuous power spectral density at the output of NLP. The practical optimum prefilter in this case is shown to be a high pass filter.

Gardner [25], by simulation examine the dependance of the synchronization error variance (σ_λ^2) on the type of prefilter, at different E/N_0 conditions) and for NLP of types x^2 and $|x|$. The signal form q(t) considered by Gardner is raised cosine (allready prefiltered version of the ordinary square wave form !) and his final conclusion is that: it is not worthy to use a prefilter specially with the $|x|$ NLP. Additional simulation results are given by Luecke et al [12].

Elmoghazy et al [28], by exprimental measurement of power spectral density at the output of NLP type " delay and multiplication", and using PCM Biphase coded signal, shows that a low pass prefilter (Butterworth of 4^{th} order) contributed equally for cut-off frequencies F_c varying from 2F and 5F (F is the bit rate).

It is worthy to note that the optimum signal shaping for timing extraction is different from the optimum signal shaping for the decision circuit and even can be contradictory. Takasaki [29] proposes a method for simuttaneous optimum signal shaping.

b) Nonlinear Processor (NLP)

The NLP can be classified as: (i) NLP without memory, such as square (x^2) and absolute value $/x/$ types (ii) NLP with memory such as a delay-multiplier type ($x\,x_\Delta$).

The NLP produces at its output the required line spectral component impeded in a noise background. The noise background originates from two sources: the input signal-noise interaction, the input noise-noise interaction and the continous spectrum of the output PCM signal itself. The continous spectrum is called "pattern noise" or self noise and the corresponding clock synchronization error is called pattern jetter, the name pattern commes from the fact that such "noise" depends on the composition of the "1" , "0" pattern of the PCM signal at the NLP input. The quantative contribution of the pattern noise on the synchronization error is given by Gardner [25] . In low E/N_s operating conditions ($E/N_0 < 12$ dB) the effect of "pattern noise" can be neglected with respect to other noise sources.

c) The Band-Pass Filter (BPF)

The BPF central frequency is F (bit rate) or nF, (in this case a frequency devider by n follows the BPF).

The PLL is used intead the PBF for several convinient reasons [25-chapter 4]. The

one, shortcoming of the PLL is its property of hanging up on random occasions. PLL occusionally exhibit unduly prolonged phase transients during initial acquisition of lock. The loop appears to stick temporarly, at a larg value of phase error befor setting to its normal tracking condition of small error. This phenomenon is called the "hang-up" effect [25].
The BPF(or the PLL) bandwidth choise is a trade -of between synchronization error and acquisition time.
The threshold of BS based on nonlinear processing is relativly high(E/N_0 minimum in the order 2 dB [28])compared to that of closed loop realizations such as the DTTL. From the other hand the acquisition time can be made as small as several bit durations, using a first order PLL [30].

III - IMPLEMENTATION TECHNIQUES

The implementation techniques can be classified as (a) analoge (b) discrete and (c) digital. Bs such as those discussed in section II and the closed loop realizations derived from MAP estimation technique can be realized.

by analoge circuits. Digital implementations are also possible for the same cited BS's. For example Elmoghazy et al [28, 30] realised a BS with NLP type delay and multiplier using exclusivly digital IC's. The DTTL is realized in one time using cabled logics [19,20]and in another time using microprocessors [31].
BS's such as those proposed by Hirchler [22] and Show [24] are adapted to implementation using microprocessors.
In digital implementations the circuits speed limits the maximum used PCM bit rate, F.

Charge coupled devices (CCD) [32] accepts at its input signals in discrete form (not quantized) and the processing speed is that of analoge circuits. Waggener [33] used commercially available CCD in implementation of a suboptimum closed loop BS derived from the MAP Optimum BS.

IV CONCLUSION:

This review paper presents the state-of-art of different building methods as well as implementation techniques of self bit synchronizers for PCM signals. The methods are classified into two, however in both methods an inherent nonlinear processing exists. This paper can be considered as a useful guide to engineers working in the field of bit synchronization of PCM signals.

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